P2001,0325

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applic. No.	:	10/701,058 Confirmation No. 5559
Applicant	:	Holger Sedlak, et. al.
Filed	:	November 4, 2003
Title	:	Frequency Regulating Circuit
Group Art Unit	:	2836
Examiner	:	Dru M. Parries
Docket No.	:	P2001,0325
Customer No.	:	24131

REPLY BRIEF

Mail Stop Appeal Brief - Patents
Hon. Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

S i r :

This is a *Reply Brief* responding to the *Examiner's Answer* dated January 3, 2008.

Remarks:

Appellants reallege and incorporate herein by reference the arguments made in their Brief on Appeal, filed on October 15, 2007.

Further, Appellants comment as follows with respect to the *Examiner's Answer* dated January 3, 2008:

In item (10) of the Examiner's Answer, pages 4 - 5, the Examiner stated, in part:

> Regarding the underlined limitations, Durham DOES teach suppressing individual clock pulses, via pulse filter (1-7, 10-13, 20; in particular 7), generated by a clock signal generator (27), in response to a control signal at the pulse filter's control input (new_data of registers 10-13) from the control device (21, 14 - 17)(Fig. 1A&B). **Durham also teaches a sensor 18 which detects the level of electrical current and determines if a "high power condition exists", and if so, it suppresses individual clock pulses until the high power condition ceases to exist (Col. 1, lines 55 - 59; Col. 6, lines 24-52).** [emphasis added by Appellants]

Appellants respectfully disagree with the statement in the Examiner's Answer that alleged that **DURHAM** disclosed **suppressing individual clock pulses** until a detected high power condition ceases to exist. More particularly, Appellants' independent claims 1 and 4 require, among other limitations,

> **said pulse filter suppressing an individual clock pulse of said clock signal generated by said clock**

> **signal generator, in response to said control signal at said control input,** such that said control device adjusts said clock frequency to provide at said output, at any time, the maximum possible clock frequency corresponding to a maximum permissible current consumption of the circuit. [emphasis added by Appellants]

Similarly, Appellants' independent claim 7 requires, among other limitations:

> **said pulse filter filtering out individual clock pulses of said clock signal generated by said clock signal generator, in response to said control signal at said control input,** such that, said control device adjusts said clock frequency to provide at said output, at any time, the maximum possible clock frequency corresponding to a maximum permissible current consumption of the circuit. [emphasis added by Appellants]

However, among other limitations of Appellants' claims, the **DURHAM** reference does **not** teach or suggest **suppressing/filtering out individual clock pulses of the clock signal generated by the clock signal generator, in response to a control signal at the pulse filter's control input,** as required by Appellants' independent claims. Rather, col. 1 of **DURHAM**, lines 55 - 59, cited in the Office Action, merely disclose:

> Generally, the frequency of the clocked signal is reduced (or increased) incrementally based upon the output of the sensor which detects the level of a specific circuit characteristic, such as heat generated, electrical current utilized, or the like.

Additionally, col. 6 of **DURHAM**, lines 24 - 52, cited in the Office Action, state:

> In this case, AND gate 7 will output a system clock signal which is identical to the oscillator clock frequency, because the oscillator clock signal and data output of the shift register will always be active and output the oscillator clock at the same frequency as the system clock, which is considered state level 4. In the case where sensor 18 has determined that a high power condition exists, the $power_{13}$ high signal is provided to synchronization latches 14 and 15. Then, control state machine 16 receives a control signal from latches 14 and 15 indicating the existence of the high power condition. Select signals are then issued by state machine 16 to pattern generator 17 **so that a bit pattern corresponding to state level 3 can be provided by pattern generator 17.** At this time, **a 0111 bit pattern output from pattern generator 17 and a 0010 is issued to the 4 bit shift register.** That is, a zero is input as the new_data in registers 10, 11 and 13. A logical one is input to register 12. The logical zero input to register 10 will cause a logical 1 to be output on the data_out port of register 10 and input to the old_data port of register 11. A logical 0 is then output to register 12 and a logical one is input to register 13 such that the logical zero is output from register 13 to AND gate 7. It can be seen that the logical zero will occur 25% of the time, since 1 of the 4 bit characters causes a logical zero to be present at AND gate 7. Thus, for every fourth cycle, the active portion of the oscillator clock is negated and the system clock output on node 20 will run at an effective clock frequency of 75% of the oscillator clock. This is at state level 3.

As can be seen from the forgoing portions of **DURHAM** cited in the Examiner's Answer, the device disclosed by **DURHAM** effectively multiplies a clock signal **with a pattern generated by a pattern generator (Fig. 1B, 17).** In **DURHAM**, a pattern generator may determine that **one of a fixed sequence of pulse**

is suppressed, for example one in every four pulses. See, for example, col. 6 of **DURHAM**, lines 46 - 51. However, **negating one out of four clock pulses by means of generating a bit pattern and loading it into a loadable shift register**, as disclosed in **DURHAM**, **does not constitute a pulse filter suppressing/filtering out individual clock pulses**, as required by Appellants' claims. Rather, in contrast to **DURHAM**, Appellants' claims require, among other limitations, a pulse filter that suppresses/filters out an individual clock pulse whenever a high power condition exists and does not filter out a clock pulse whenever the high power condition does not exist.

Further, page 5 of the Examiner's Answer states, in part:

> The Examiner would like to note that the Appellant's arguments, on page 11 of 17, stating that his claims require or state "the pulse filter is directly controlled by the control signal" and "an individual pulse is filtered out whenever the control signal is provided" and "the filter suppresses an individual pulse, directly in response to the receipt of control signal" have no basis. That is, the claims do not specifically state any of these limitations, particularly the underlined statesments. [emphasis in the original]

Appellants' respectfully disagree. More particularly, Although parts of the terms "**directly controlled**", "**whenever**" and "**directly** in response" are not explicitly recited in Appellants' pending independent claims, it is clear from each

claim, when considered in its entirety, that a one-to-one relationship between the (instantaneously measured) consumption of the circuit configuration and the filtering of an individual clock pulse is required and recited by the claims. For example, Appellants' independent claims require, among other limitations:

> . . . said control device providing a control signal to said control input of said pulse filter **when** said means for comparing determine that the instantaneous current consumption exceeds the definable threshold value; [emphasis added by Appellants]

As such, the control signal of Appellants' claims is provided **when** (i.e., "whenever") the means for comparing determines that the instantaneous current consumption exceeds the definable threshold value.

Additionally, Appellants' independent claims 1 and 4 further recite, among other limitations:

> **said pulse filter suppressing an individual clock pulse** of said clock signal generated by said clock signal generator, **in response to said control signal at said control, such that said control device adjusts said clock frequency to provide** at said output, **at any time**, the maximum possible clock frequency corresponding to a maximum permissible current consumption of the circuit. [emphasis added by Appellants]

Appellants' independent claim 7 recites a similar limitation, among others. Although the term "directly" is not explicitly

stated in those claims, the subsequent clarification that the "control device adjusts said clock frequency to provide at said output, **at any time**, the maximum possible clock frequency corresponding to a maximum permissible current consumption of the circuit" clearly recites and expresses that, in Appellants' claimed invention, **the pulse suppression stops as soon as the current consumption sinks below the predefined threshold vaule**. Thus, these claims describe and require the pulse filter to be **directly controlled** by the control signal, contrary to the Examiner's allegations. In Appellants' claimed invention, that the maximum possible clock frequency corresponding to a maximum permissible current consumption of the circuit is maintained at all times provides considerable advantages over the prior art arrangement taught by **DURHAM**.

Additionally, page 5 of the Examiner's Answer additionally alleged, in part:

> Regarding, the Appellant's argument stating that Durham teaches a multitude of control signals instead of one control signal, please note that Durham teaches a more in-depth diagram than what the Appellant discloses in his application. The Appellant's lack of detail in not showing more than one signal being sent during the process of determining current being above a threshold and suppressing a clock pulse cannot serve as a basis for attacking the more complete circuit diagram disclosed by Durham.

Contrary to the above-allegation, Appellants' solution, as presented in the present application, does not lack detail

with respect to the circuit arrangement of **DURHAM**. On the contrary, Appellants' disclosure is believed to provide proper and sufficient disclosure of all required circuit componets of the claimed frequency regulating circuit. It is a further advantage of the present invention that no additional circuitry is required to implement it. In particular, and in contrast to in **DURHAM**, no loadable shift register, no pattern generator and no further control circuitry is required.

Further still, contrary to the allegation on page 6 of the Examiner's Answer, Appellants maintain that it would not be obvious to a person of ordinary skill in the art to combine the prior art documents of **DURHAM** and **WANG**, in the manner suggested in the Office Action. More particularly, because **DURHAM** is only faced with the question of determining **an average** current consumption for a given number of clock pulses (for example, for four subsequent clock pulses), **DURHAM** has no need for an **instantaneous** current detector, as disclosed by **WANG**. For this reason alone, it would not be obvious to a person of ordinary skill in this art to combine the teachings of **DURHAM** and **WANG**, which teachings also pertain to different areas of technology, as previously discussed in Appellants' Appeal Brief.

For the foregoing reasons, among others, Appellants' claims

are believed to be patentable over **DURHAM** and **WANG**, whether taken alone or in combination. The Honorable Board is therefore respectfully urged to reverse the final rejection of the Primary Examiner.

Please charge any fees that might be due with respect to Sections 1.16 and 1.17 to the Deposit Account of Lerner Greenberg Stemer LLP, No. 12-1099.

Respectfully submitted,

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For Appellants

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